REMARKS

In view of the above amendments and following remarks, reconsideration and further examination are requested.

Initially, a replacement formal drawing for Figure 4 is provided herewith which includes a lead line that correctly identifies upper metal layer 29a.

The specification and abstract have been reviewed and revised to make editorial changes thereto and generally improve the form thereof, and a substitute specification and abstract are provided. No new matter has been added by the substitute specification and abstract.

Claims 1-7 have been amended and claims 8-19 have been added.

The currently pending claims are believed to be free of the 35 U.S.C. § 112, second paragraph, issue raised by the Examiner. In this regard, please note that amended claim 4 recites that the external electrodes and the metal plate are --co-planar--. The specification has been correspondingly amended. None of the claims recite a "virtual plane". Accordingly, it is respectfully submitted that the currently pending claims are in compliance with 35 U.S.C. § 112, second paragraph.

The instant invention pertains to a semiconductor apparatus that is to be used for ultra-high frequency signal processing or high-speed optical communication. Such a semiconductor apparatus is generally known in the art, but suffers from drawbacks as expressed on pages 1-2 of the original specification. Applicant has addressed and resolved these drawbacks by designing a unique semiconductor apparatus.

With reference to Fig. 2, for example, the inventive semiconductor apparatus comprises a semiconductor device 12, a first dielectric board 13a surrounding the semiconductor device, a second dielectric board 13b surrounding the semiconductor device and on the first dielectric board, a metal cover 15 on the second dielectric board and above the semiconductor device, external electrodes 18, upper wiring 17a on the second dielectric board, first through-hole wiring 17c penetrating the first dielectric board and electrically connected with the external electrodes, second through-hole wiring 17d penetrating the second dielectric board and electrically connected with the upper wiring, and internal wiring 17b between the first dielectric board and the second dielectric board. The

semiconductor device 12 is connected with the external electrodes 18 via the first through-hole wiring 17c and the internal wiring 17b, and the first through-hole wiring 17c and the second through-hole wiring 17d are electrically connected with the internal wiring 17b while being away from each other. Amended claim 1 is to be representative of Applicant's inventive semiconductor apparatus.

Claims 1, 3, 6 and 7 were rejected under 35 U.S.C. § 102(b) as being anticipated by Hung et al., claim 2 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Hung et al. in view of Karnezos, and claims 4 and 5 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hung et al. in view of Adachi et al. These rejections are respectfully traversed, and the references relied upon by the Examiner are not applicable with regard to the amended and newly added claims for the following reasons.

Claim 1 has been amended to include the additional limitation of **upper wiring on the second dielectric board, wherein the second through-hole wiring is electrically connected with the upper wiring**. This upper wiring is shown in Fig. 2 as reference numeral 17a, in Fig. 4 as reference numeral 27a and in Fig. 5 as reference numeral 37a. Hung et al. does not disclose or suggest such upper wiring. Please note that this limitation was present in originally filed claim 3.

In rejecting claim 3, towards the bottom of page 3 of the Office Action the Examiner sates that Hung et al. shows

> an upper wiring arranged on the second dielectric board and
> connected with the second through-hole wiring [through microstrip 112].

However, it is respectfully submitted that such upper wiring is lacking from Hung et al. In this regard, Applicant has studied Hung et al., and it is not seen as to how this reference can be said to include the upper wiring as now recited in claim 1. That is, microstrip 112 can possibly be said to correspond to upper wiring; however, this microstrip is connected only to the semiconductor device 110 and is not connected with the second through-hole wiring 126. Accordingly, it is respectfully submitted that amended claim 1 is not anticipated by Hung et al. None of the other references resolve this deficiency of Hung et al., and accordingly, claim 1 is also allowable over any possible combination of the references relied upon by the Examiner.

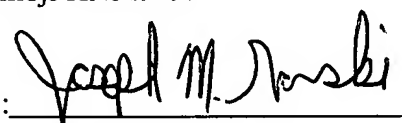
If the Examiner continues to assert that Hung et al. does disclose the upper wiring as now recited in claim 1, then the Examiner is respectfully requested to specifically identify that member of Hung et al. that corresponds to this wiring.

In view of the above amendments and remarks, it is respectfully submitted that the present application is in condition for allowance and an early Notice of Allowance is earnestly solicited.

If after reviewing this Amendment, the Examiner believes that any issues remain which must be resolved before the application can be passed to issue, the Examiner is invited to contact the Applicant's undersigned representative by telephone to resolve such issues.

Respectfully submitted,

Tomoji HAMADA

By: 

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AMENDMENTS TO THE DRAWINGS:

Replacement Formal Drawing for Figure 4 has been filed concurrently.